UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/088,913 | 05/07/2002 | Michael O. Thompson | 3672-0144P | 8909 |

2292 7590 09/21/2005

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

| EXAMINER | |
|---|---|
| HUR, JUNG H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2824 | |

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/088,913 | THOMPSON ET AL. | |
| | Examiner | Art Unit | |
| | Jung (John) Hur | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *6-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,12 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05 July 2005 (along with After-Final Amendment, filed 25 February 2005) has been entered.

### *Amendment*

2. Acknowledgment is made of applicant's Amendment, filed 05 July 2005, along with After-Final Amendment, filed 25 February 2005. The changes and remarks disclosed therein have been considered and entered.

No claims have been cancelled or added. Therefore, claims 1-13 are pending in the application. Of these, claims 6-11 remain withdrawn from further consideration as being drawn to non-elected inventions.

### *Allowable Subject Matter*

3. The indicated allowability of claims 2-5 are withdrawn in view of the newly discovered reference to Dierke. Rejections based on the newly cited reference(s) follow.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709).

Kuroda, for example in Figs. 1 and 2, discloses a non-volatile passive matrix memory device comprising ferroelectric memory cells (for example, C0 - C7 in Fig. 2); word lines (for example, W00 - W07 in Fig. 2) and bit lines (for example, D0 - D7 in Fig. 2) that are orthogonal to each other; the word lines divided into a number of segments (for example, BLOCK (0,0) through BLOCK (0,7) in Fig. 1), each segment comprising and being defined by a plurality of adjoining bit lines (for example, D0 - D7 for BLOCK (1,0)); each word line in a segment is differentiated based on the position of the word line within the segment (i.e., in different row positions), each word line in the segment being adjoined to a separate bit line (i.e., in a matrix structure); a plurality of sensing means (for example, SA in WRC0 - WRC7), each being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line (see, for example, column 12, lines 42-54).

However, Kuroda does not disclose means for connecting each separate bit line assigned to a segment with an associated sensing means, such that the world line of the same position within each segment is sensed at the associated sensing means, thus enabling simultaneous

connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment.

Clemons, for example in Figs. 2 and 3, discloses means (for example, via T200 - T203 controlled by BYTE BLOCK DECODER) for connecting each separate bit line (for example, bit lines for columns C11 - C14) assigned to a segment (for example, BYTE BLOCK 1) with an associated sensing means (for example, SA1 - SA4 via I/O SWITCHES in Fig. 3), such that the world line of the same position (i.e., a selected word line) within each segment is sensed at the associated sensing means, thus enabling simultaneous connection of all memory cells (for example, M111 - M114) assigned to a word line (for example, R1) on a segment (for example, BYTE BLOCK 1) for readout via the corresponding bit lines (for example, bit lines for columns C11 - C14) of the segment.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the device of Kuroda by incorporating the means of Clemons for connecting each bit line assigned to a segment with an associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, as an equivalent alternative means for segmenting and simultaneously accessing a byte (or a word or other widths of bits) of information from the memory, for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43).

6. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1 above, and further in view of Dierke (U.S. Pat. No. 5,734,615).

Regarding claim 2, the combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claim 1 above, with the exception of the simultaneous connection of each bit line of a segment with the associated sensing means during addressing is accomplished by multiplexers.

Dierke, for example in Fig. 7, discloses multiplexers (42-0' through 42-7') for simultaneously connecting (since multiplexers are commonly controlled) each bit line of a segment (three segments defined by BIT 0-7, BIT 8-15 and BIT 16-23) with an associated sensing means (at the output of each multiplexer).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the multiplexing means of Dierke for the multiplexing means of Clemons, since both means are equivalent for simultaneously connecting bit lines of a segment with an associated sensing means, for the purpose of having a ferroelectric memory organization that provides for improved utilization of spare columns, while allowing for subdivision of the memory into portions (see Clemons column 3, lines 40-43), and the selection of these equivalents would be within the level of ordinary skill in the art.

Regarding claims 3-5, the above Kuroda/Clemons/Dierke combination further discloses that the number of multiplexers corresponds to the largest number of bit lines defining a segment (in Fig. 7 of Dierke, eight bit lines per segment; when adapted for Clemons with four

multiplexers; see Clemons, Fig. 2), each bit line of a segment being connected with a specific multiplexer (see Dierke, Fig. 7 in which BIT 0-7, for example, are connected to the respective multiplexers); wherein the output of each multiplexer is connected with a signal sensing means (inherent in Dierke, Fig. 7; SA1-SA4 in Fig. 3 of Clemons); wherein the signal sensing means is a sense amplifier (SA1-SA4 in Fig. 3 of Clemons).

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda (U.S. Pat. No. 5,487,029) in view of Clemons (U.S. Pat. No. 4,599,709) as applied to claim 1 above, and further in view of Seyyedy (U.S. Pat. No. 5,969,380).

The combination of Kuroda and Clemons discloses a non-volatile passive matrix memory device as in claim 1 above, with the exception of a volumetric data storage apparatus with a plurality of stacked layers, each layer comprising one of said non-volatile passive matrix memory devices. Seyyedy, for example in Figs. 1 and 2, discloses a ferroelectric volumetric data storage apparatus with a plurality of stacked layers (for example, four layers in Fig. 1 and three layers in Fig. 2), each layer comprising one of non-volatile passive matrix memory devices (planar ferroelectric memory arrays). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to stack a plurality of devices (as discloses in the above combination of Kuroda and Clemons) in a volumetric data storage apparatus, as in Seyyedy, for the purpose of increasing the density of memory cells over a given substrate area.

***Response to Arguments***

8. Applicant's arguments filed 25 February 2005 and 05 July 2005 have been fully considered but they are not persuasive.

In the arguments filed 25 February 2005, regarding claims 1, 12 and 13, Applicant argues, in the top paragraph on page 15, that, in Clemons, "[a]ll of the transistors are connected together allowing a decoder to access the transistors simultaneously for a given byte block," and asserts that "[s]imultaneous access is achieved for the byte block and not for word line across multiple segments" (emphases added by the examiner). Further, starting at the bottom of page 15, Applicant argues that "[i]n fact, Clemons teaches with regard to FIG. 3, separating portions of the memory cells and accessing these separate portions at different times, not a simultaneous [access] of all memory cells assigned to a word line, as in the present invention." These arguments appear to imply that all memory cells across multiple segments are accessed simultaneously.

In response, it is noted that claims 1, 12 and 13 recite "thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment" (emphases added by the examiner), which is supported by Figs. 5 and 6 of the present application, and does not recite nor imply a simultaneous access across multiple segments, as asserted in the arguments. Therefore, as recited in claims 1, 12 and 13 and asserted by Applicant in the arguments, Clemons teaches a simultaneous access for a byte block (or a segment).

In the arguments filed 05 July 2005, Applicant argues, in the middle of page 2, that "one of ordinary skill in the art would not look to the teachings of Clemons" because "Clemons

teaches an SRAM (static random access memory) which ... is very different from the passive matrix addressable ferroelectric memory," and continues on to present the differences between SRAMs and ferroelectric memories. Applicant further argues, starting near the bottom of page 4, that "Hence, Clemons neither addresses nor solves the problem posed by the embodiments of the present invention,...In contrast, the present invention is concerned with parallel readout [of] data words running into said kilobits in order, for example, to compensate for the slow random access time as compared with either a static RAM or dynamic RAM."

In response, it is noted that although the basic principle of operation and characteristics are different between SRAMs and ferroelectric memories, both include word lines, bit lines, decoders and sense amplifiers; further, Clemons' teachings in Figs. 2 and 3 are substantially same as the corresponding portions of the present invention recited in claims 1, 12 and 13, in that the number of sense amplifiers is same as the number of bit lines in a segment (or a block) to enable a simultaneous access of the segment (or the block). Therefore, regardless of the problem being addressed and solved by the present invention, one of ordinary skill in the art would readily recognize the advantages of Clemons' teachings and apply it to ferroelectric memories (including that of Kuroda, as well as other types of memories), for the motivation given in Clemons, thus obtaining the features recited in claims 1, 12 and 13.

### *Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Matsubara et al. (U.S. Pat. No. 5,581,503) disclose a multiplexing scheme.

Hashemi et al. (U.S. Pat. No. 5,337,414) discloses a multiplexing scheme.

Nishino (U.S. Pat. No. 5,025,419) discloses a multiplexing scheme.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

ANH PHUNG
PRIMARY EXAMINER